

FIG. 1

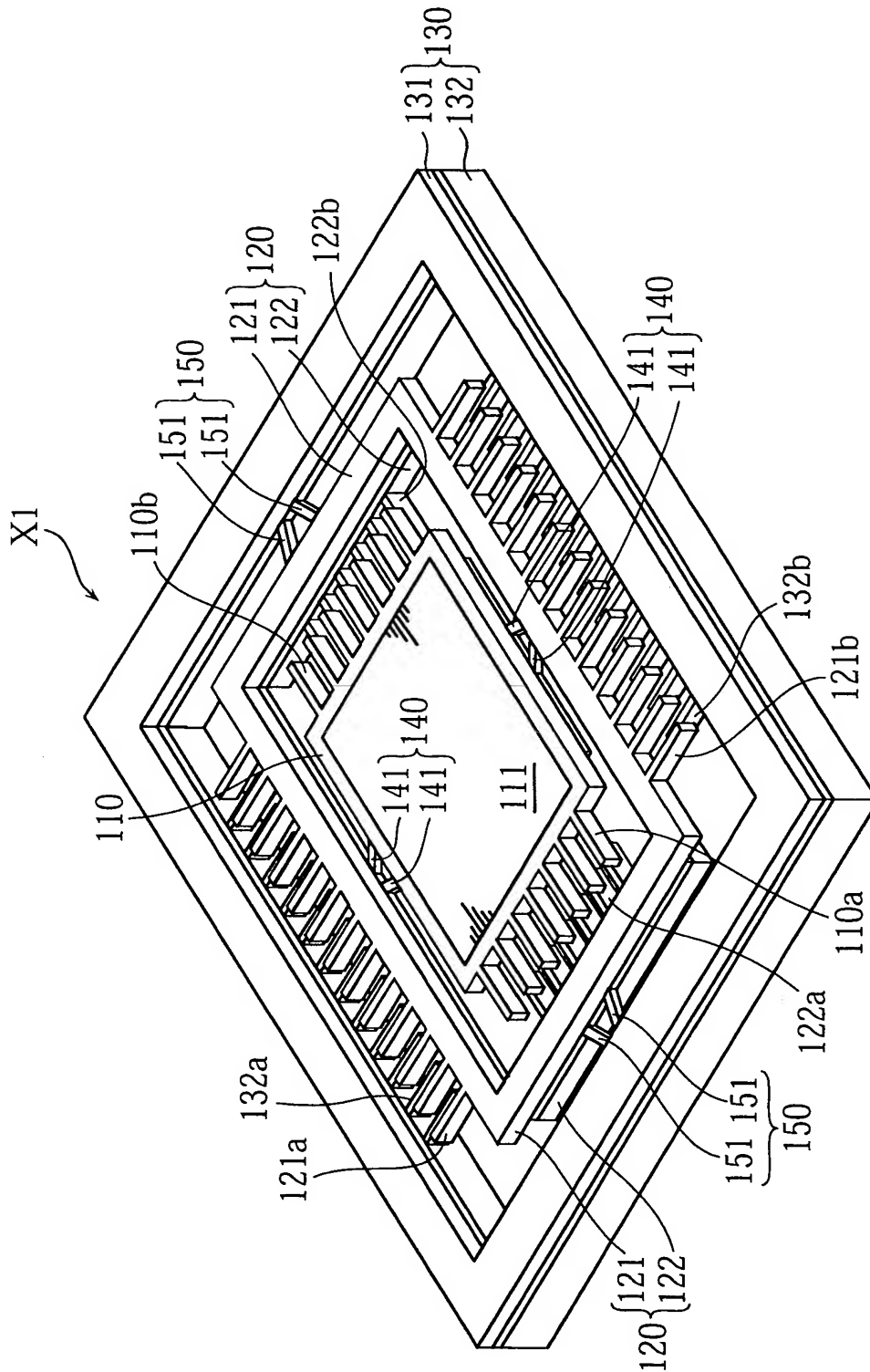


FIG. 2

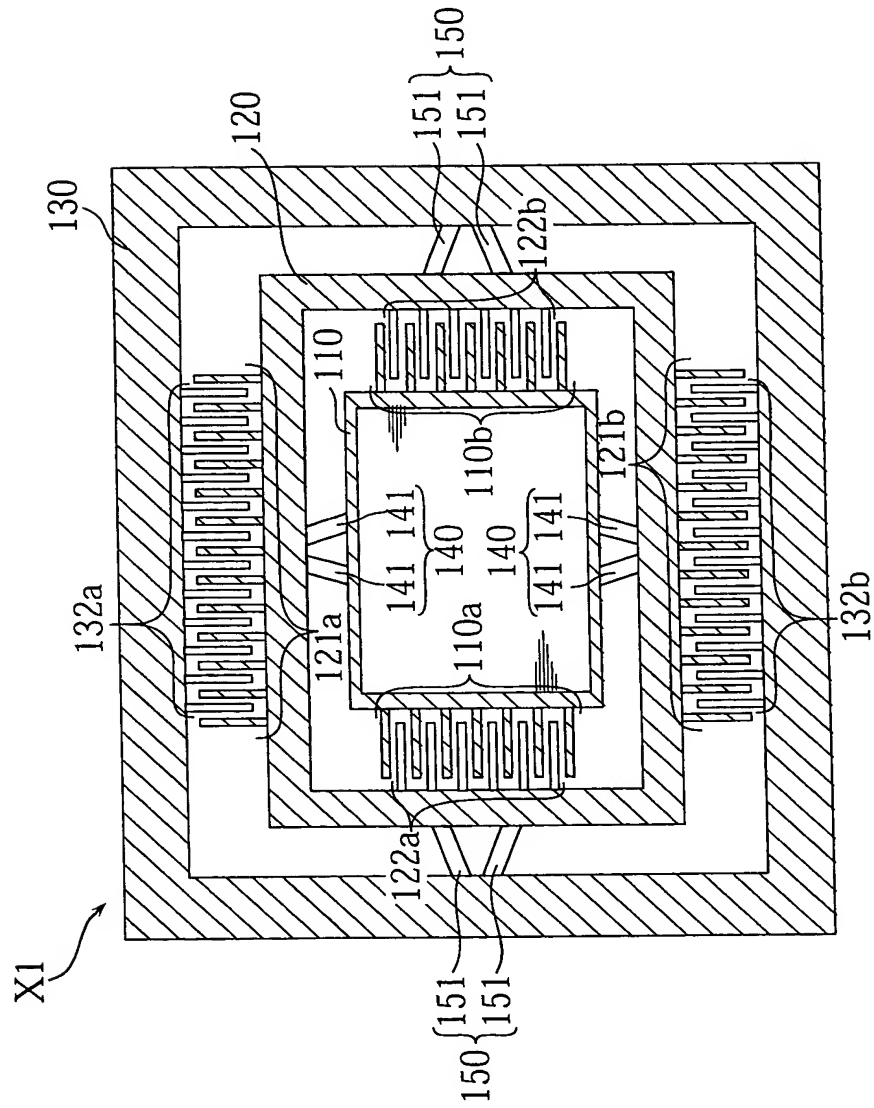


FIG. 3a

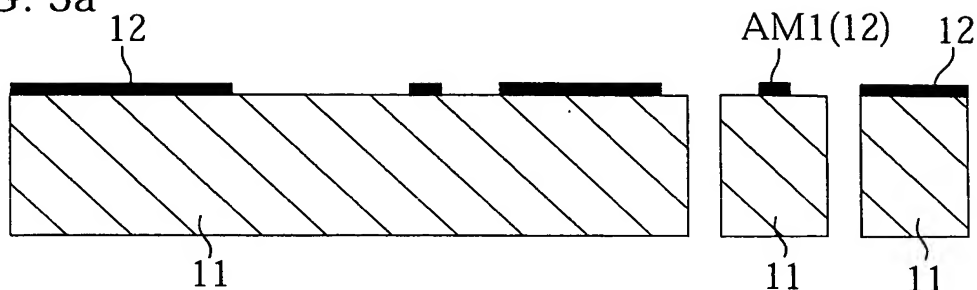


FIG. 3b

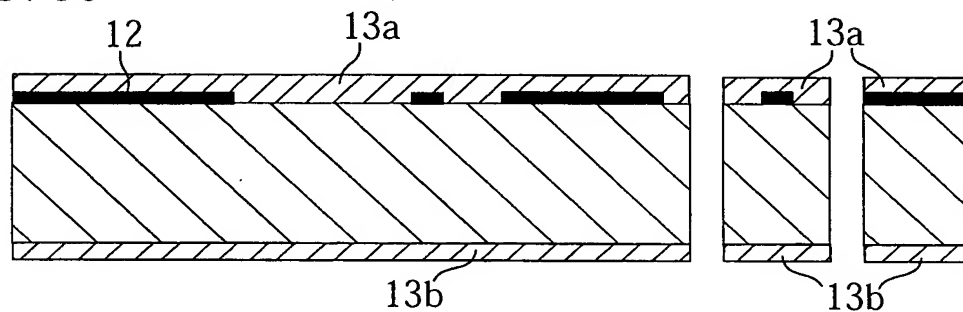


FIG. 3c

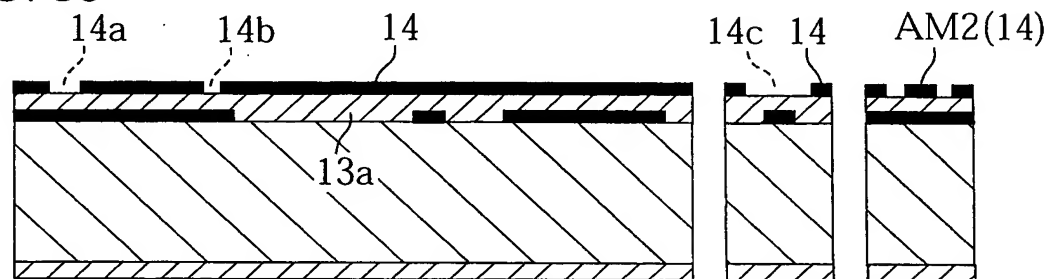


FIG. 3d

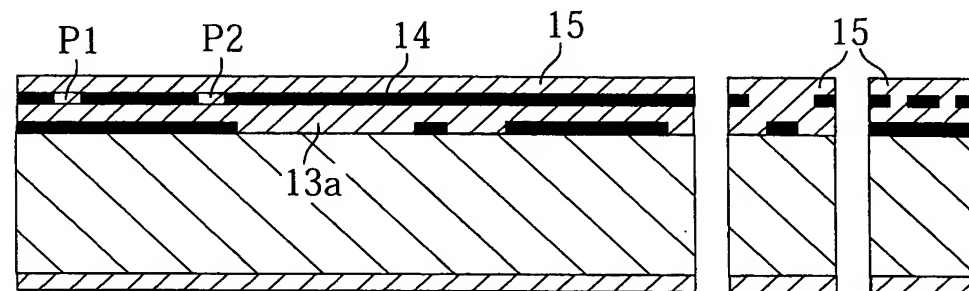


FIG. 4a

15

16

FIG. 4b

103
102
101
11
13b
14(105)
13a
12(104)
15
16

FIG. 4c

FIG. 4c is a cross-sectional view of a semiconductor device. It shows a substrate 101 with a thin layer 103 on top. A thick layer 104 is deposited on 103, and a patterned layer 11 is on top of 104. A cross-section of a trench is shown on the right, revealing layers AM1, 103, 104, and AM2.

FIG. 4d

111

103

101

17

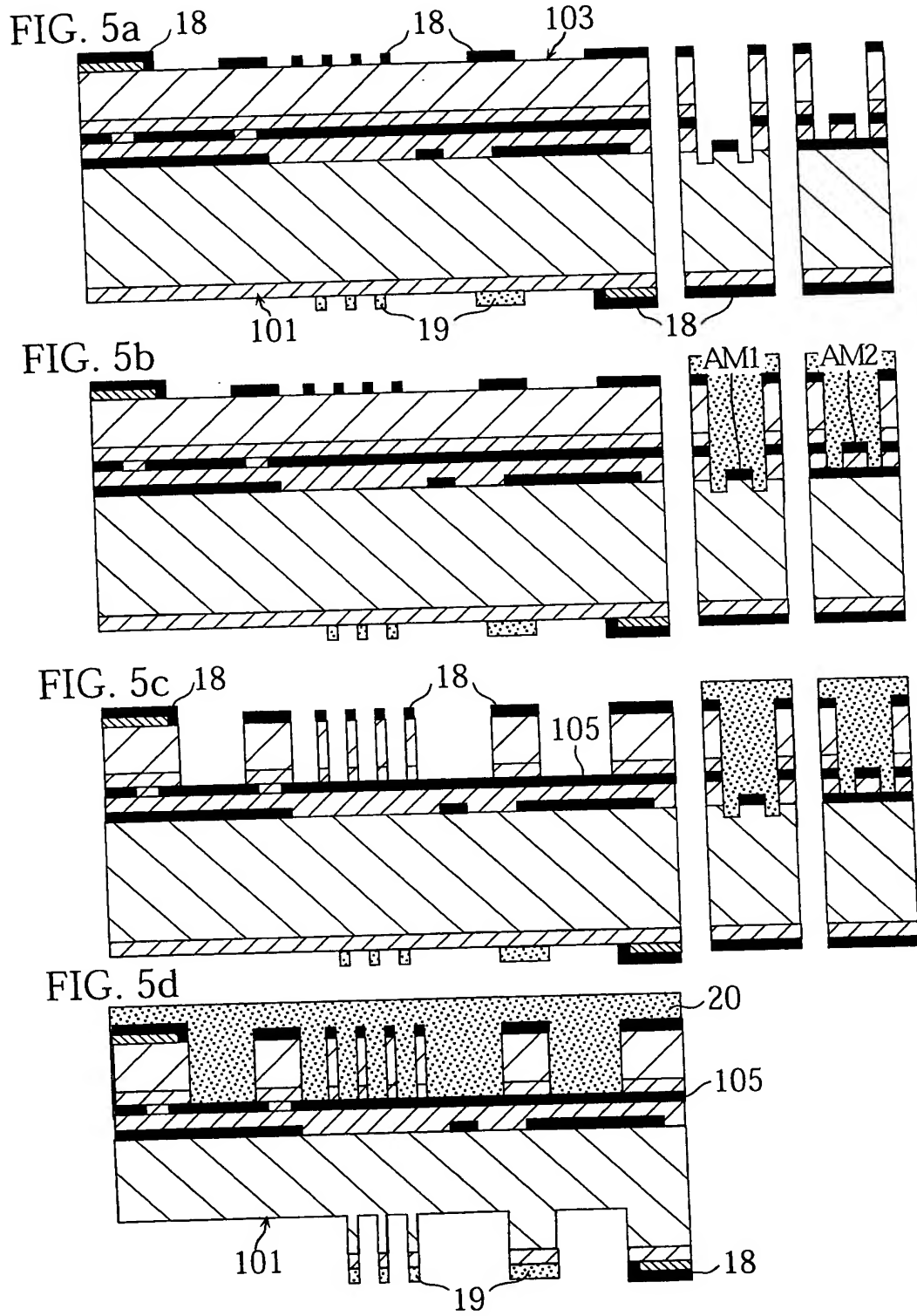


FIG. 6a

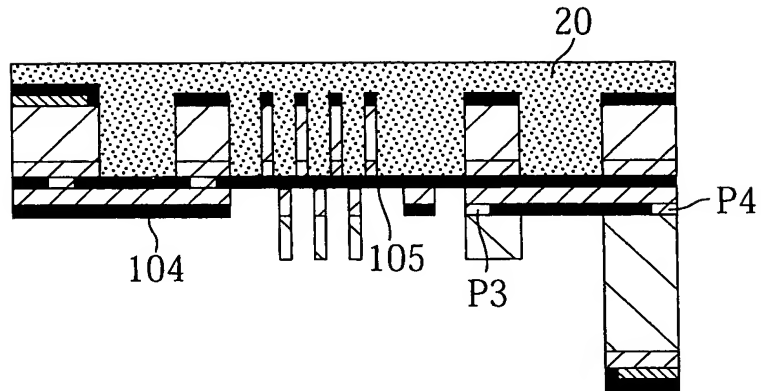


FIG. 6b

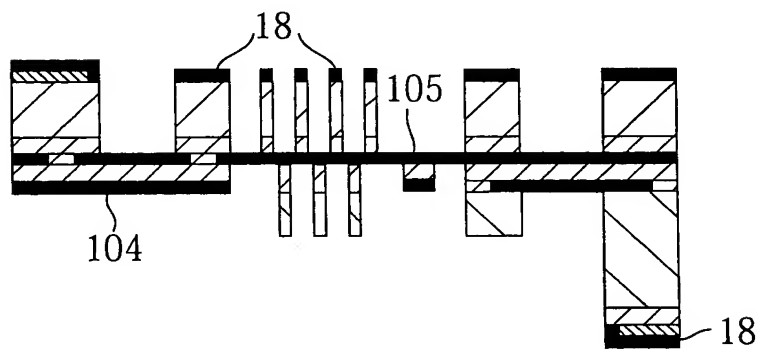


FIG. 6c

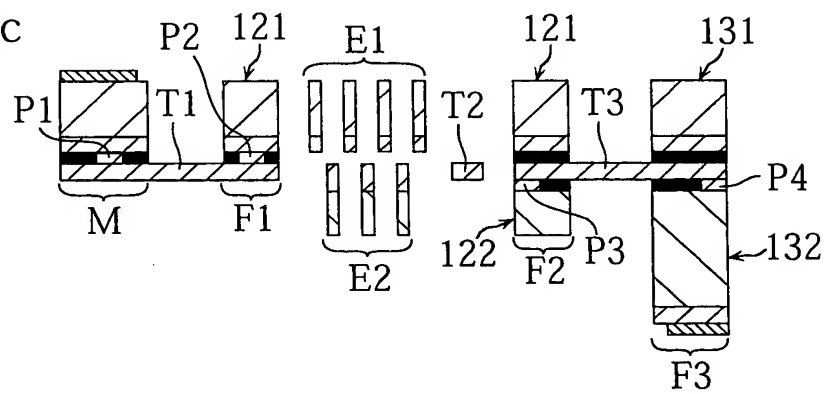


FIG. 7a

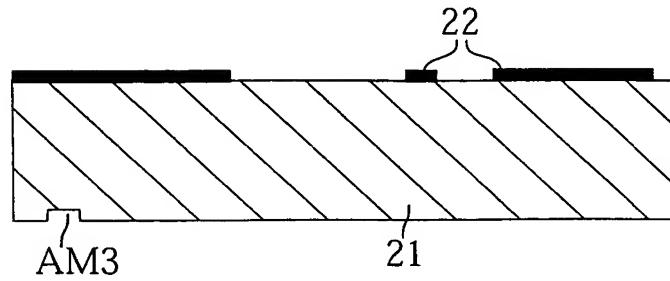


FIG. 7b

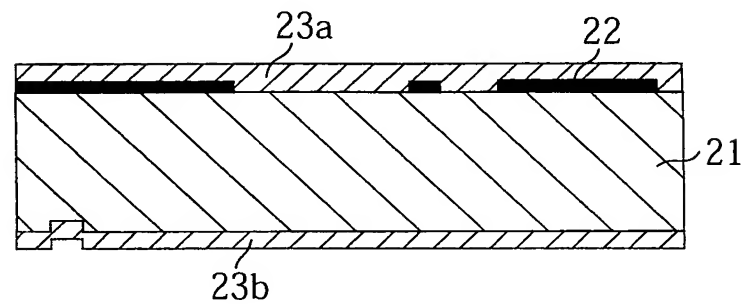


FIG. 7c

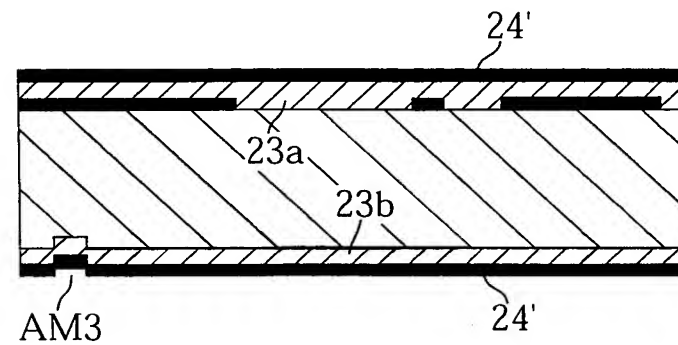


FIG. 7d

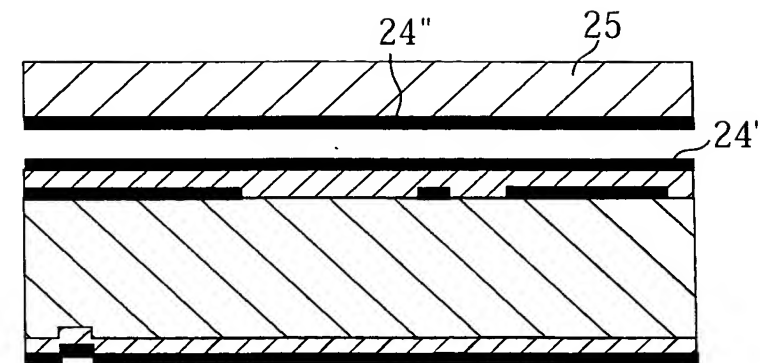


FIG. 8a

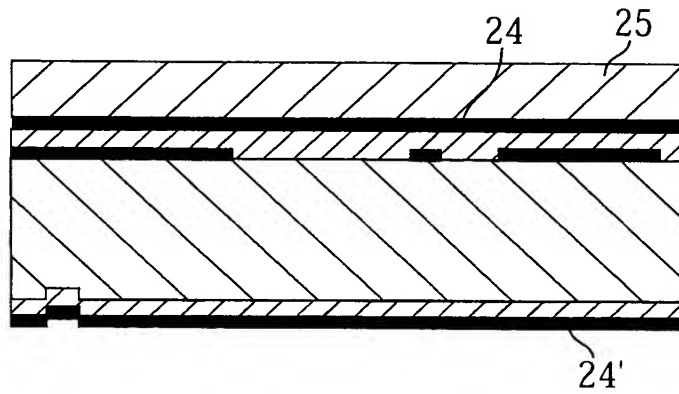


FIG. 8b

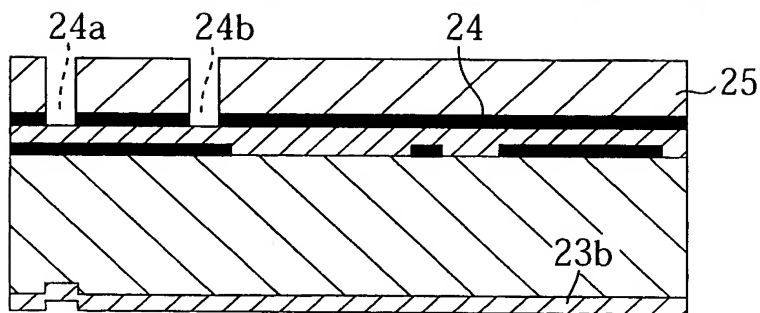


FIG. 8c

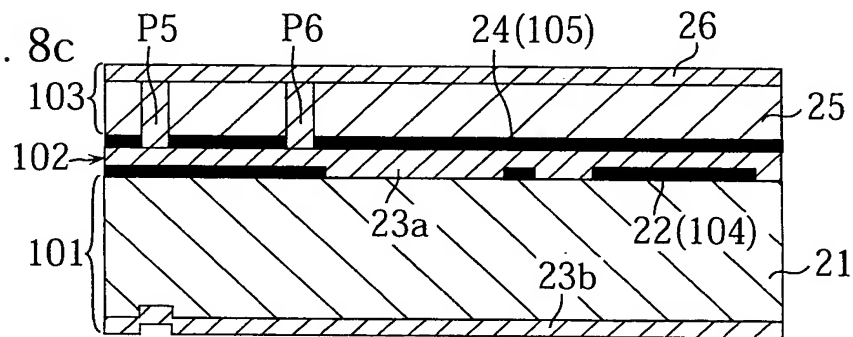


FIG. 8d

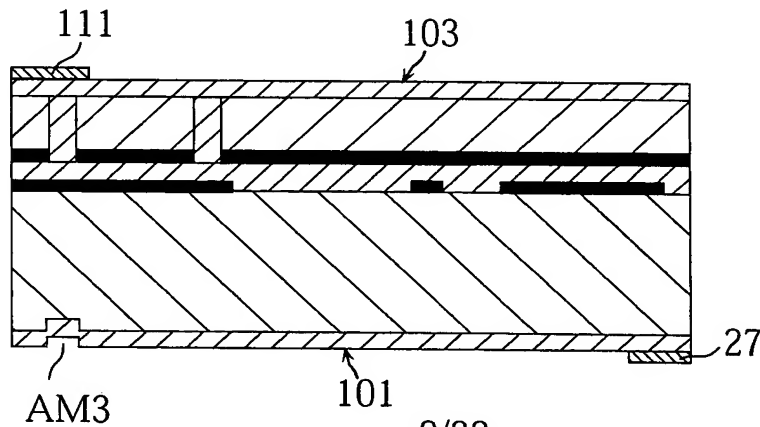


FIG. 9a

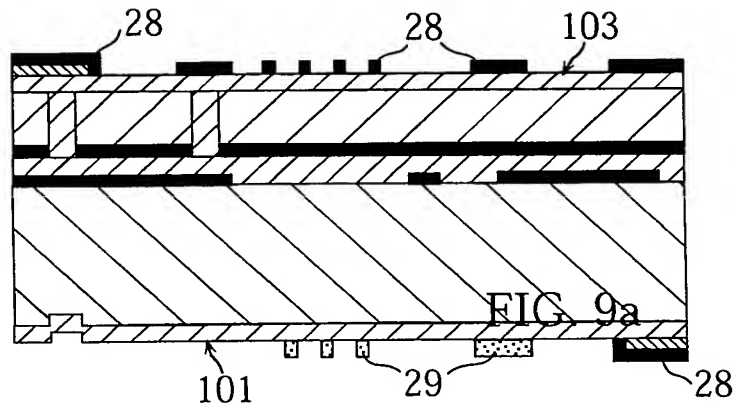


FIG. 9b

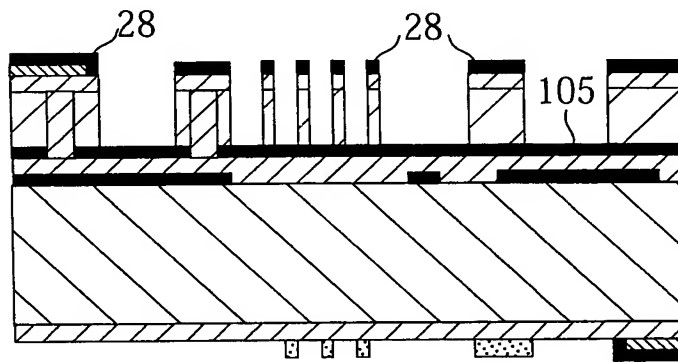


FIG. 9c

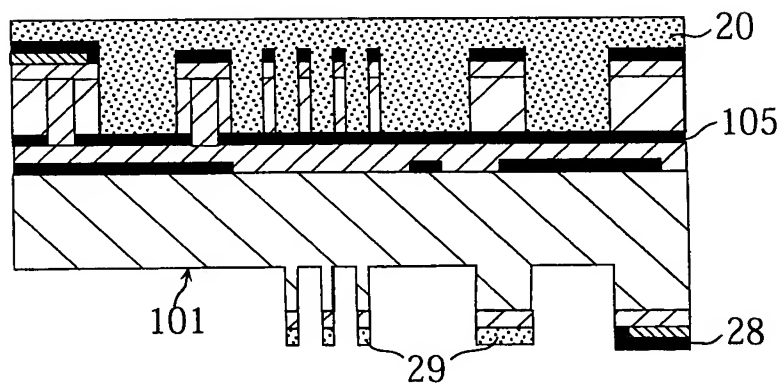


FIG. 10a

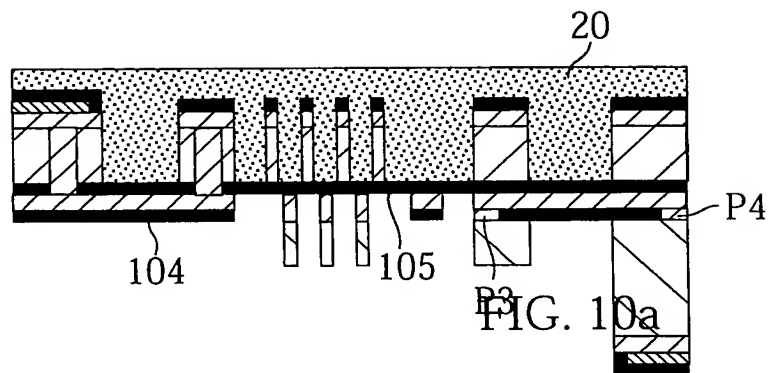


FIG. 10b

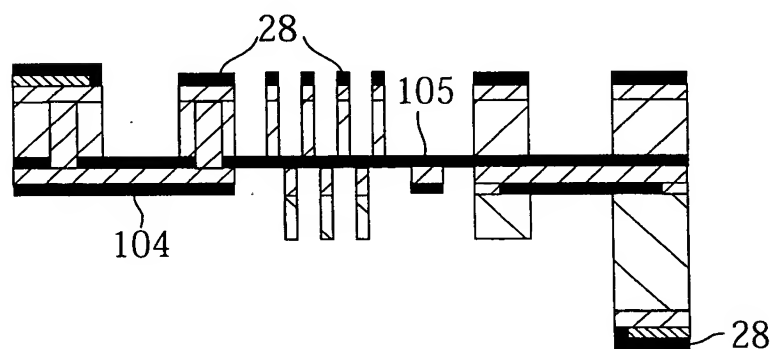


FIG. 10c

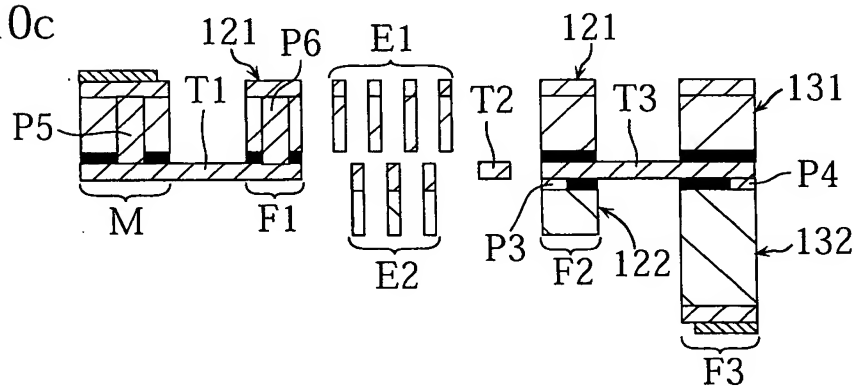


FIG. 11a

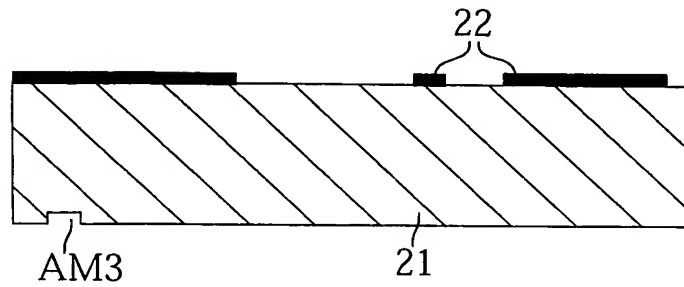


FIG. 11b

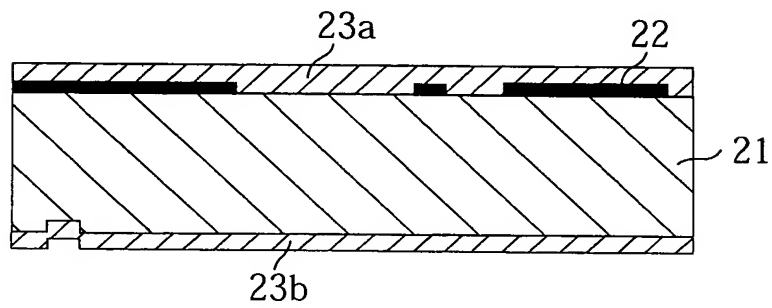


FIG. 11c

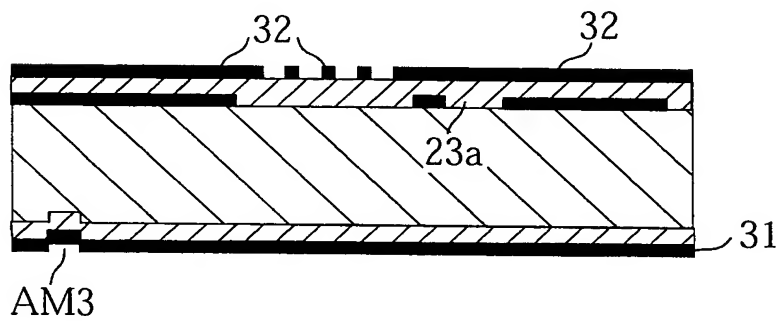


FIG. 11d

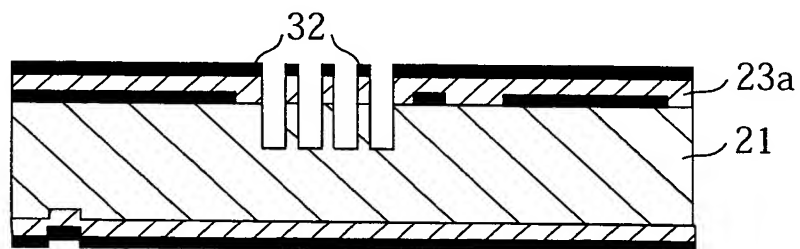


FIG. 12a

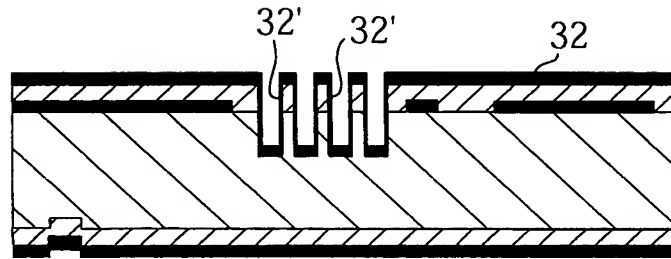


FIG. 12b

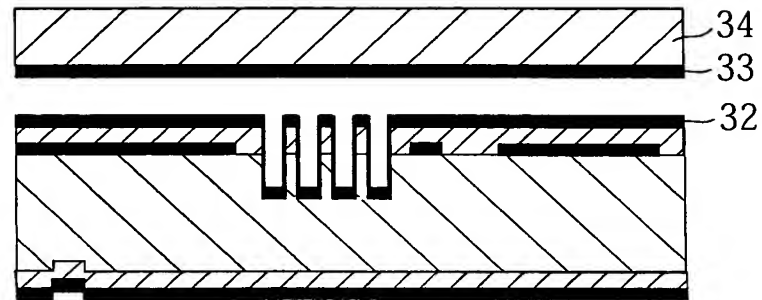


FIG. 12c

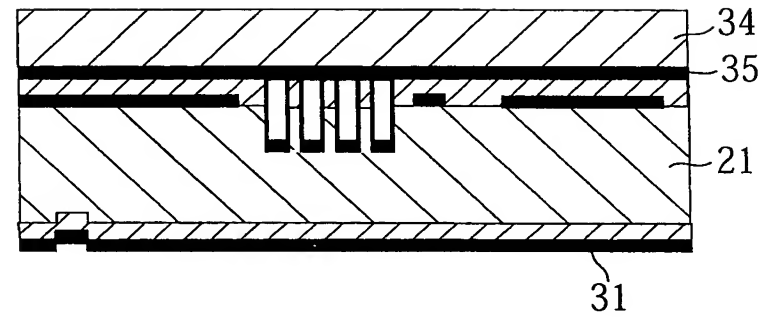


FIG. 12d

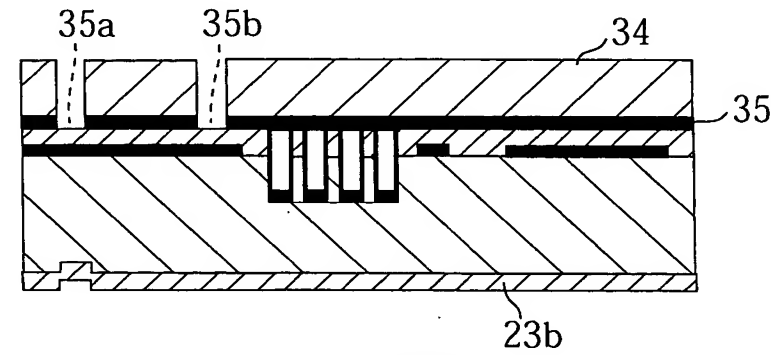


FIG. 13a

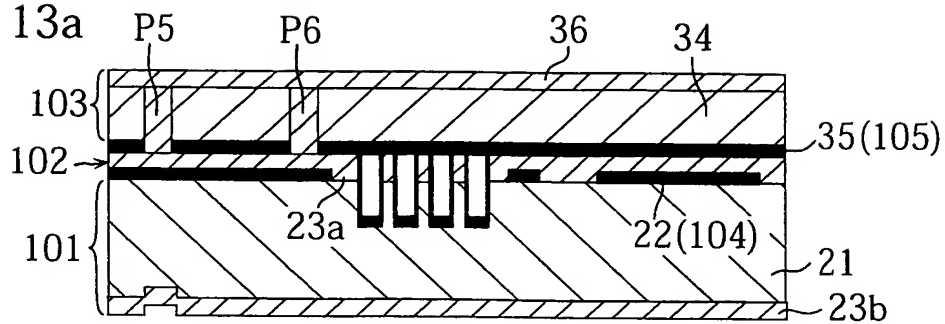


FIG. 13b

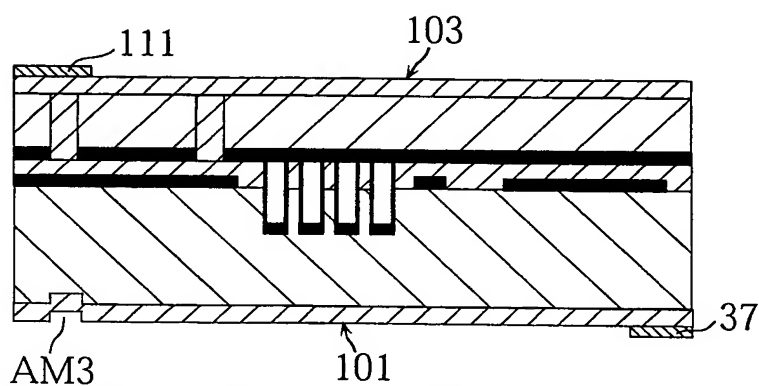


FIG. 13c

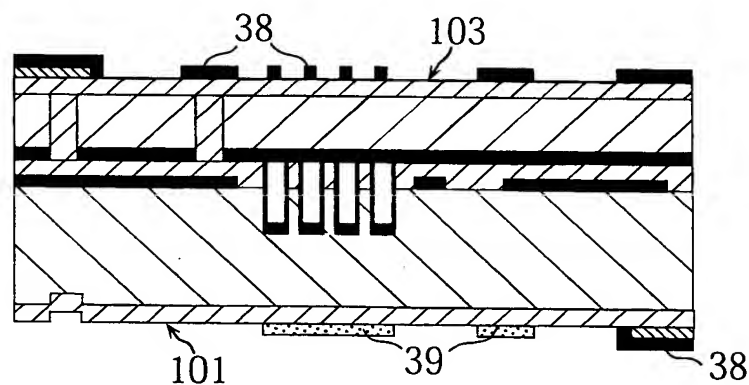


FIG. 13d

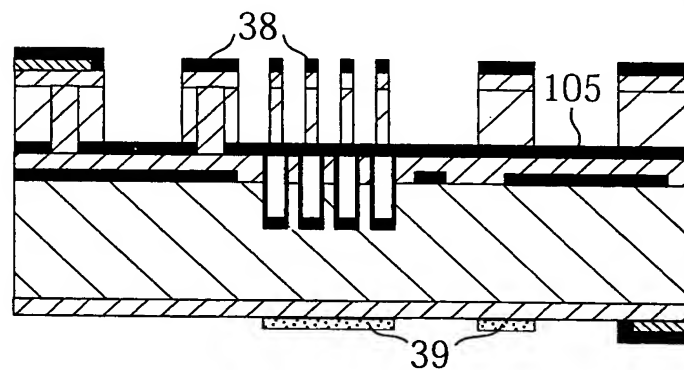


FIG. 14a

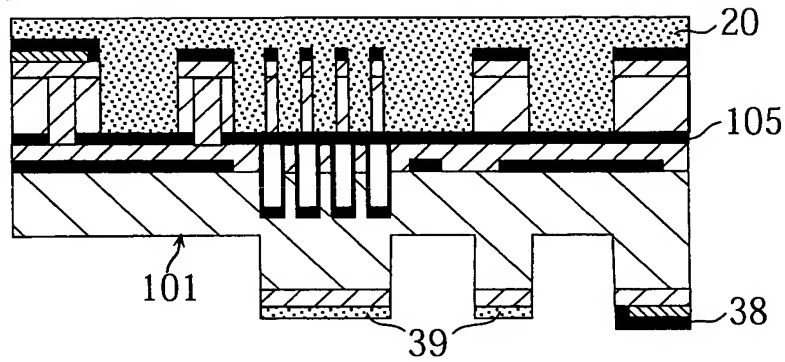


FIG. 14b

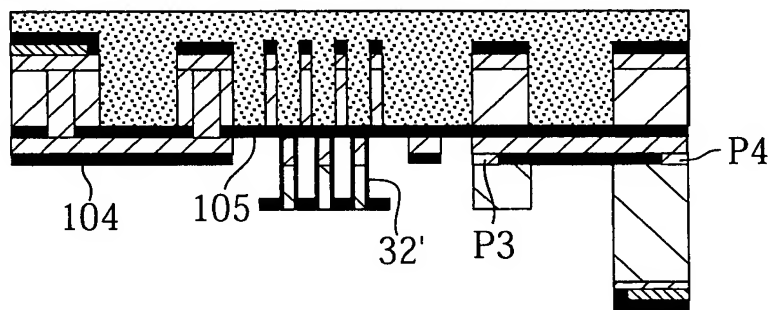


FIG. 14c

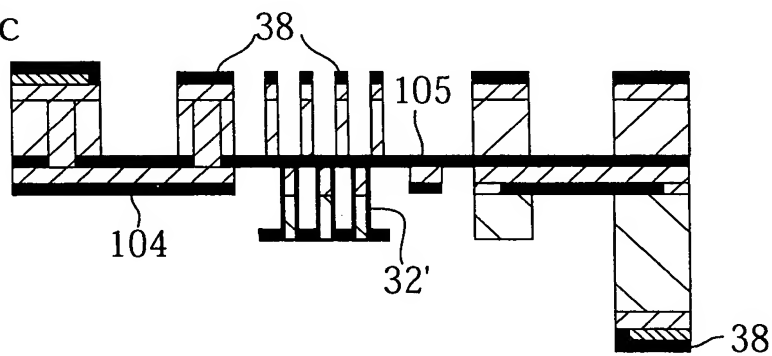


FIG. 14d

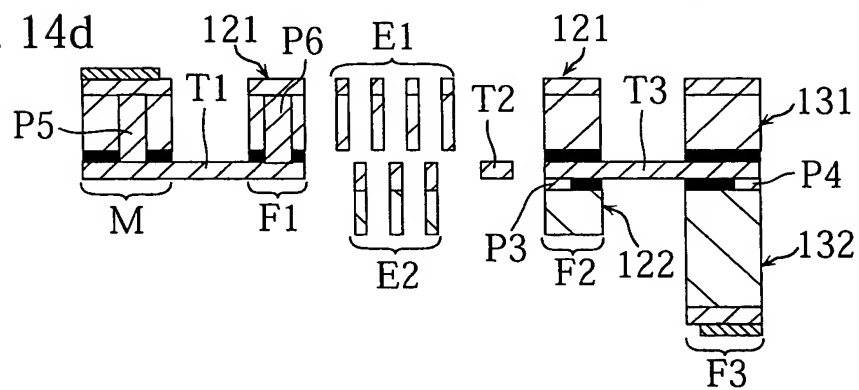


FIG. 15a

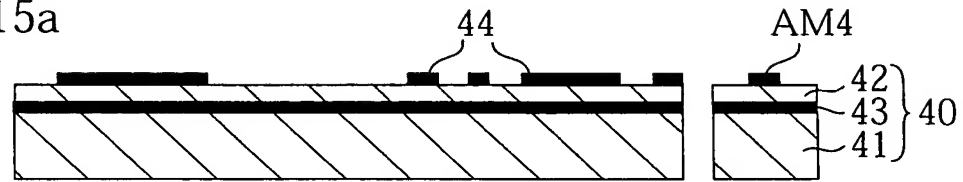


FIG. 15b

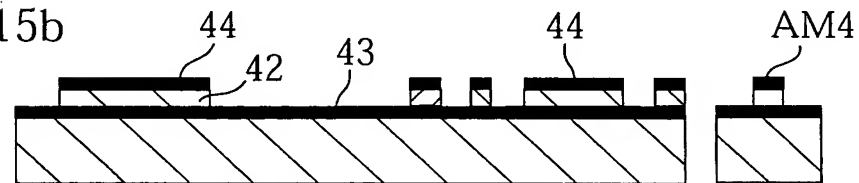


FIG. 15c

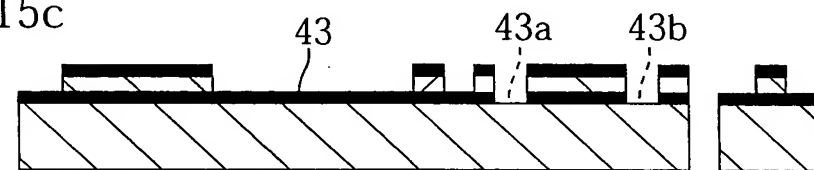


FIG. 15d

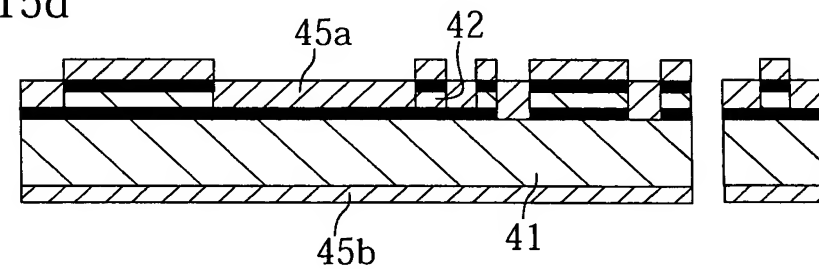


FIG. 16a

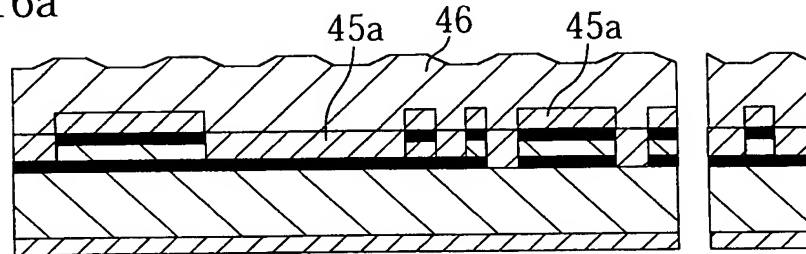


FIG. 16a

FIG. 16b

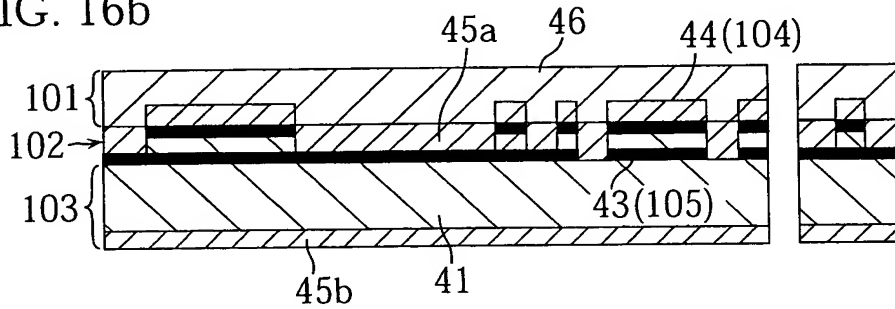


FIG. 16c

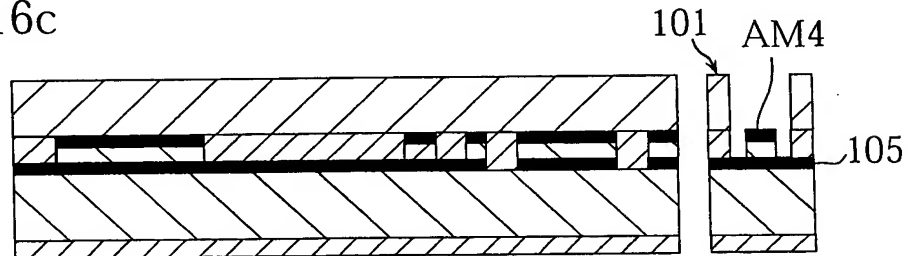


FIG. 16d

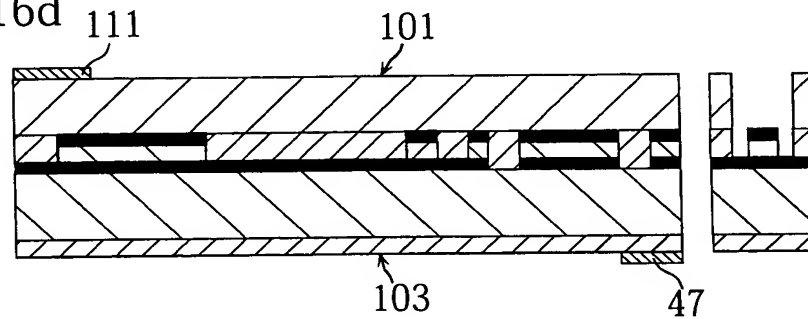


FIG. 17a

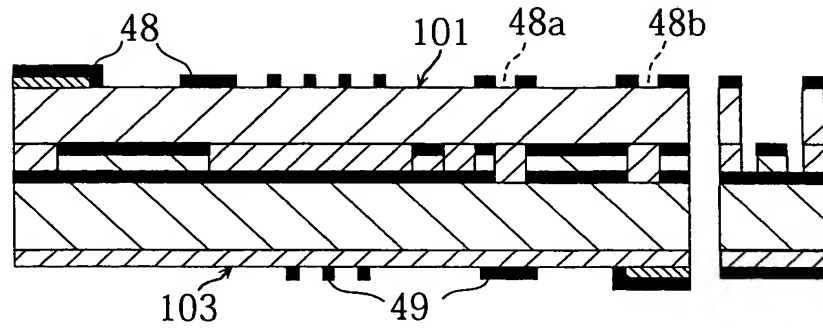


FIG. 17b

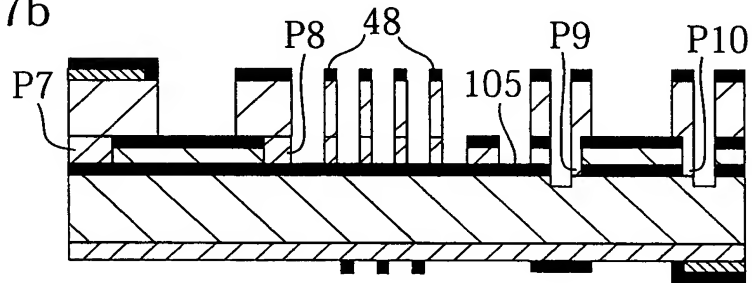


FIG. 17c

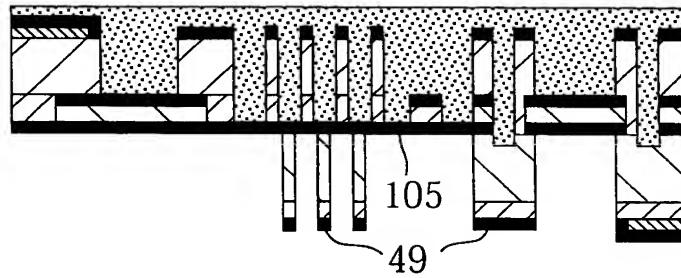


FIG. 17d

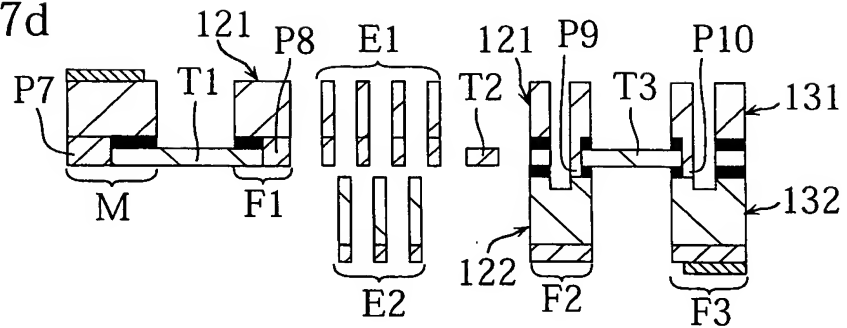


FIG. 18a

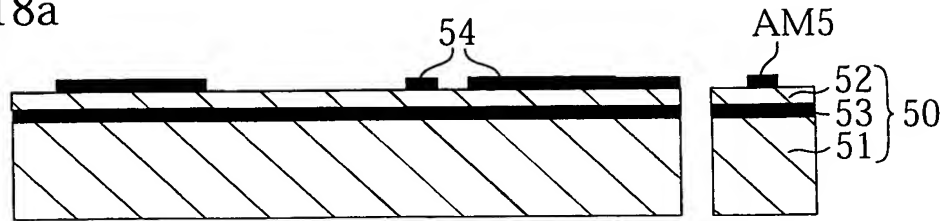


FIG. 18b

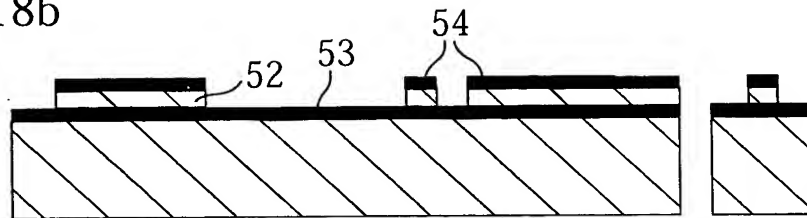


FIG. 18c

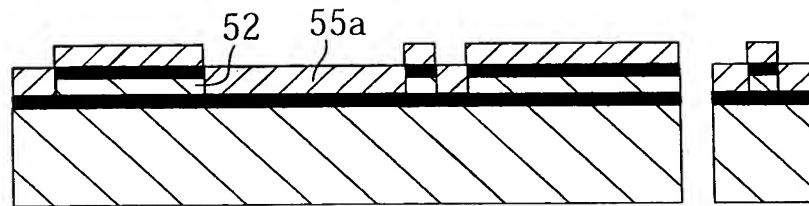


FIG. 18c

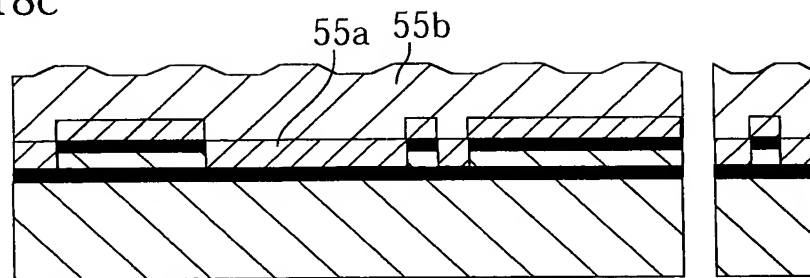


FIG. 19a

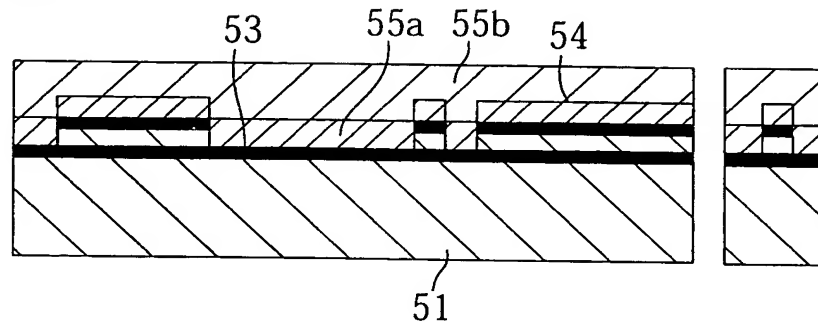


FIG. 19b

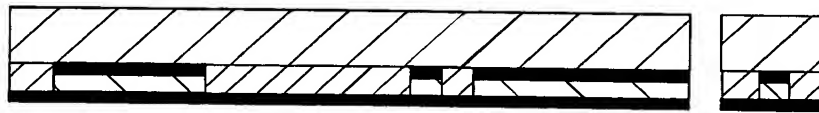


FIG. 19c

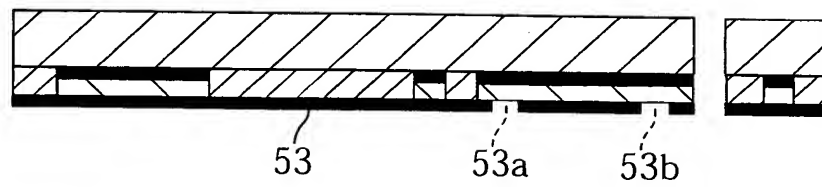


FIG. 19d

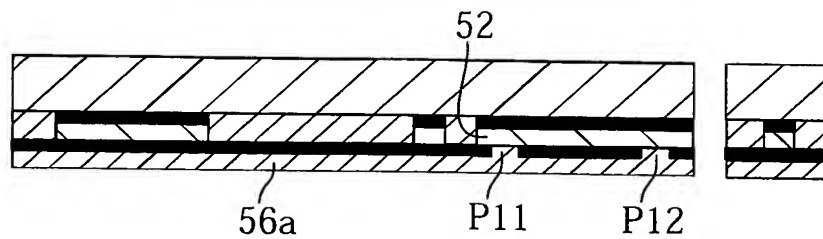


FIG. 20a

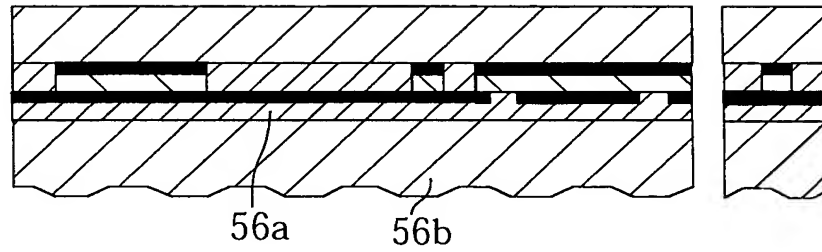


FIG. 20b

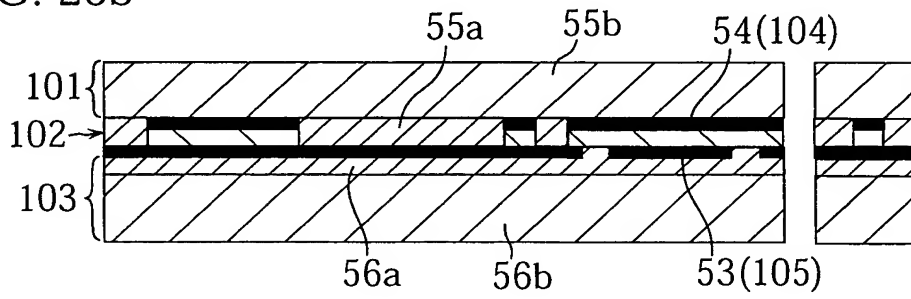


FIG. 20c

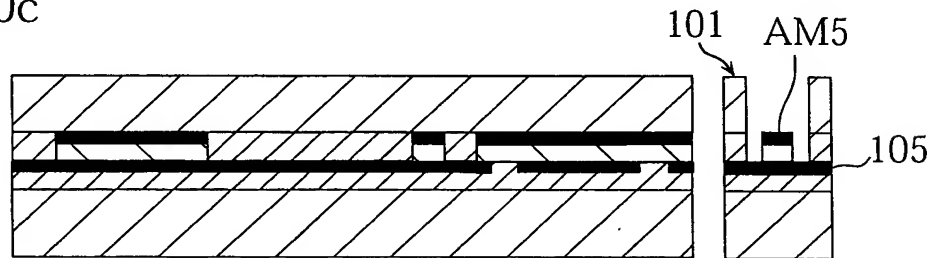


FIG. 20d

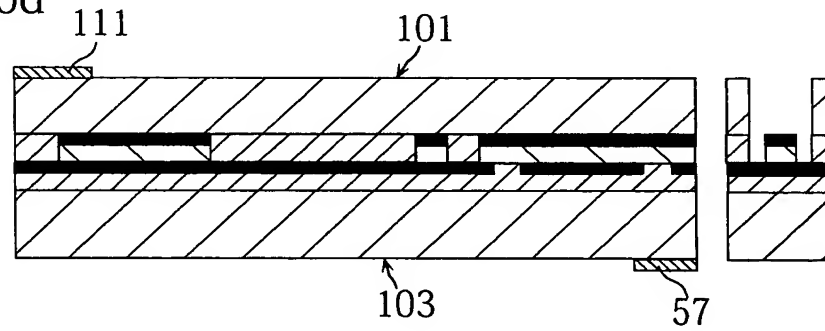


FIG. 21a

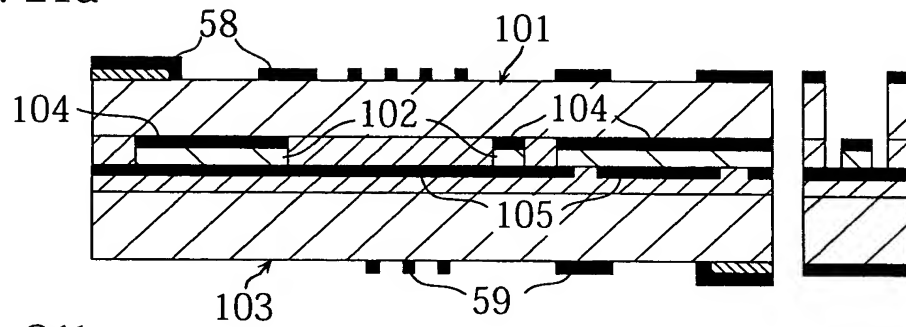


FIG. 21b

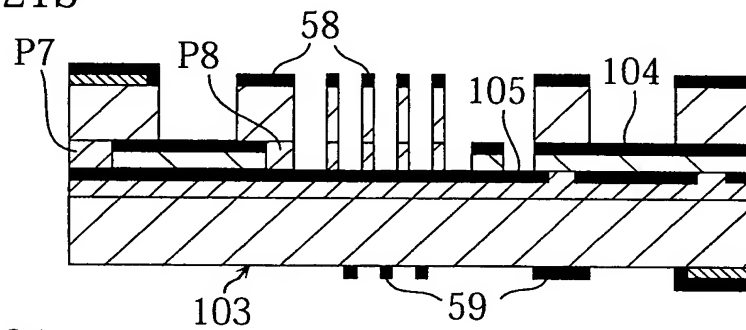


FIG. 21c

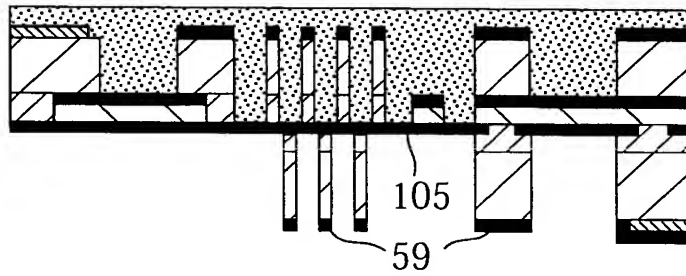


FIG. 21d

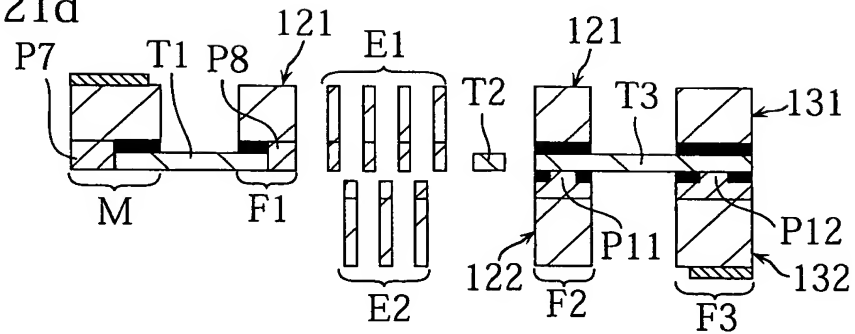


FIG. 22a

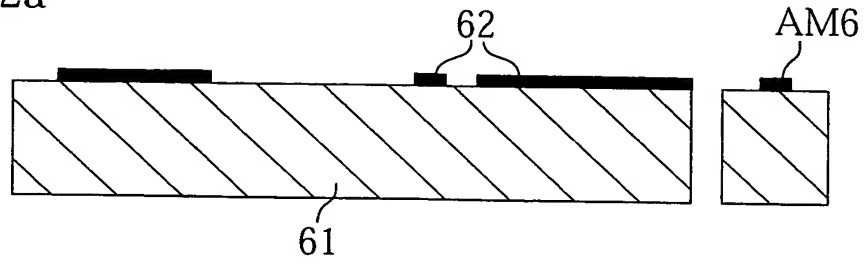


FIG. 22b

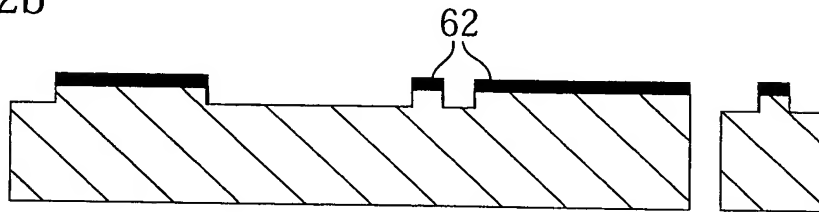


FIG. 22c

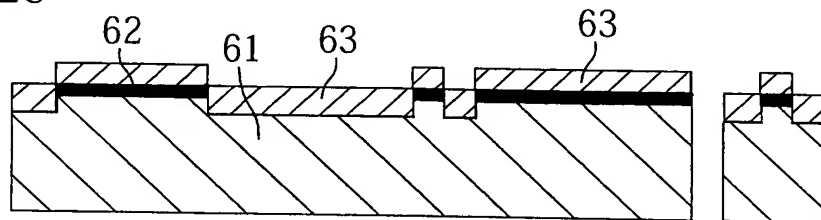


FIG. 22d

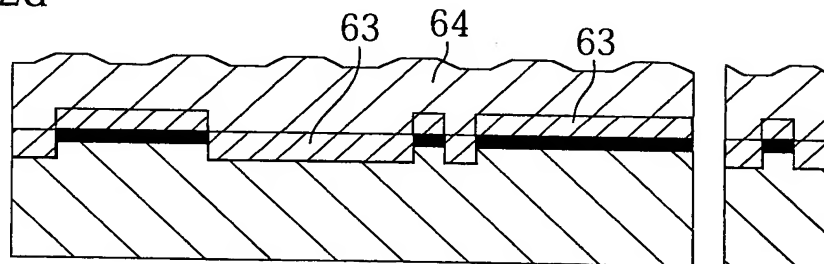


FIG. 23a

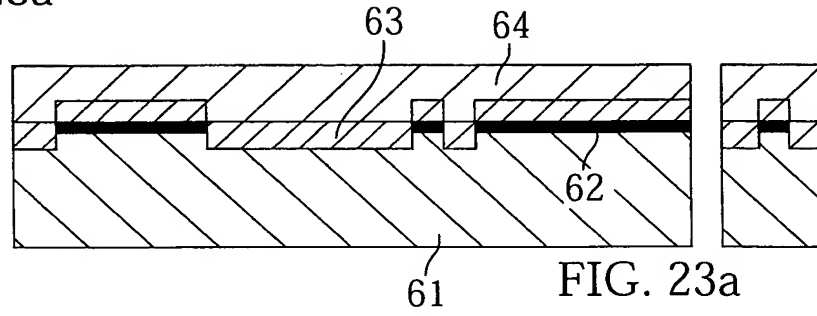


FIG. 23b

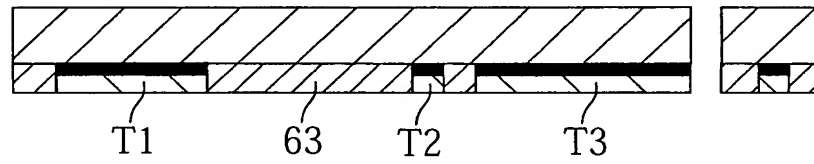


FIG. 23c

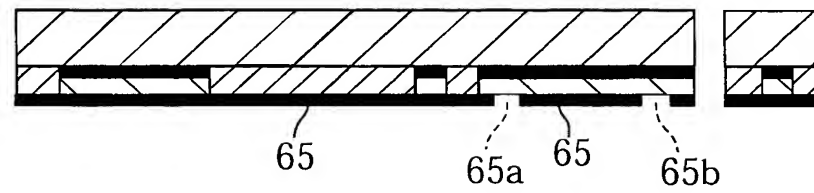


FIG. 24a



FIG. 24b

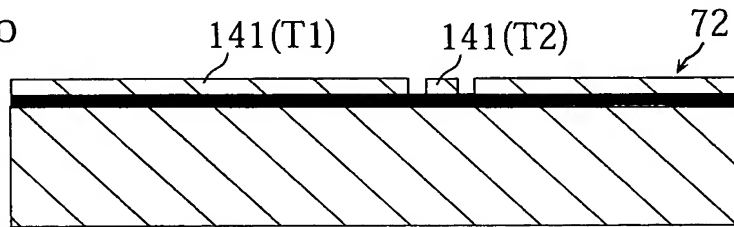


FIG. 24c

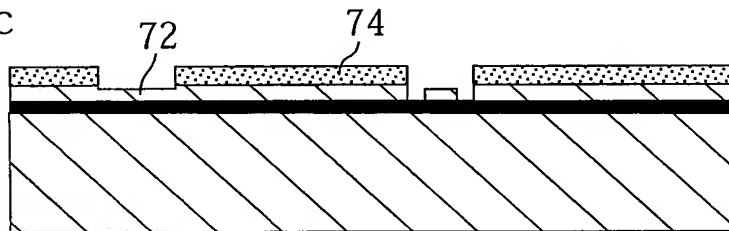


FIG. 24d

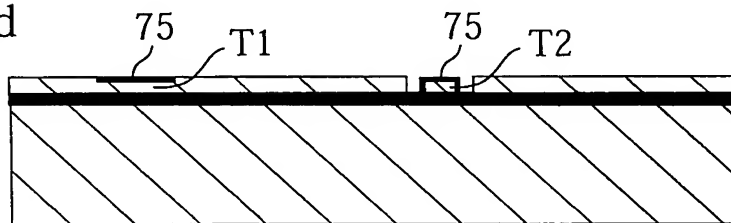


FIG. 25a

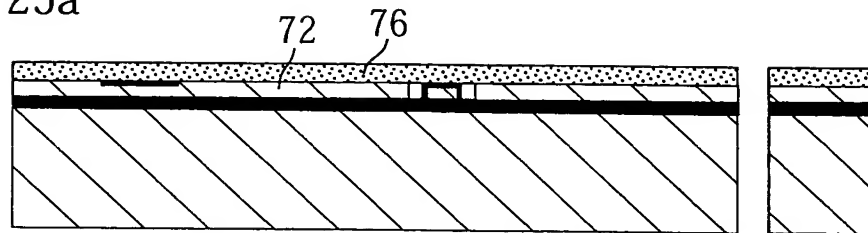


FIG. 25b

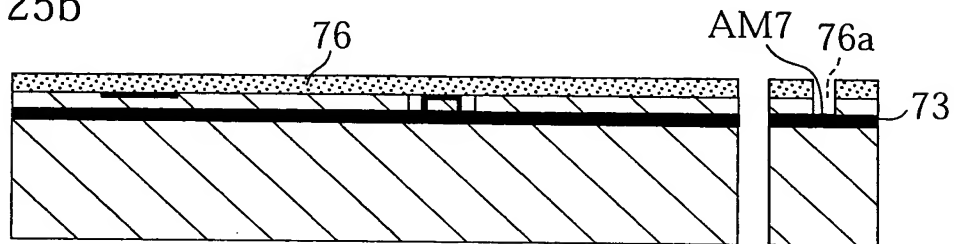


FIG. 25c

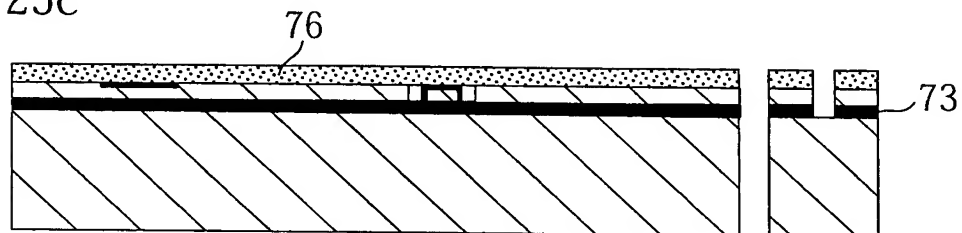


FIG. 25d

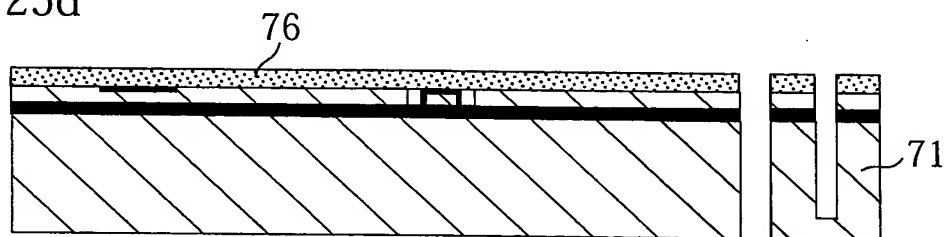


FIG. 26a

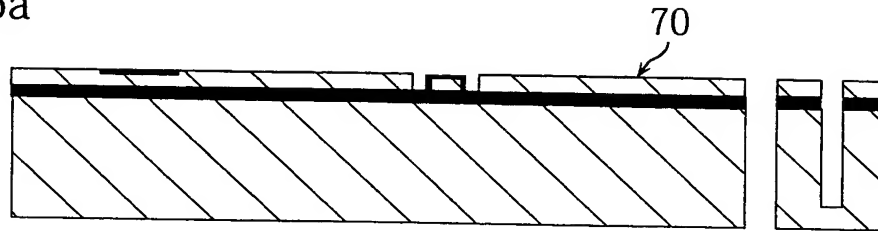


FIG. 26b

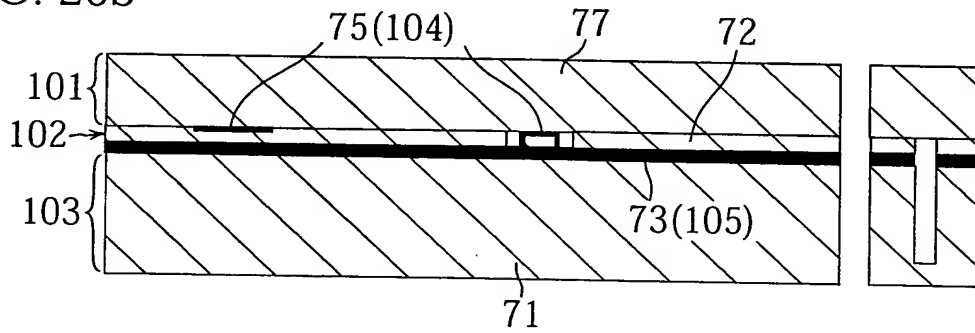


FIG. 26c

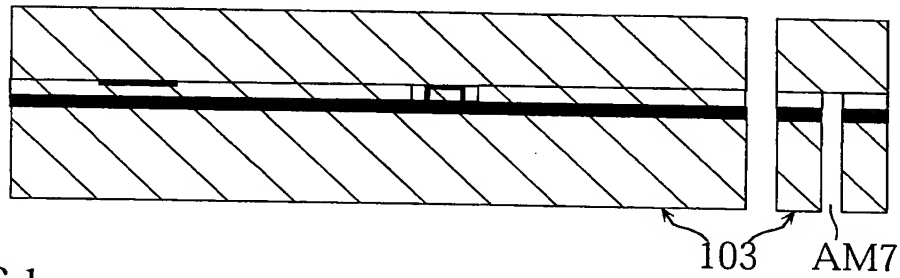


FIG. 26d

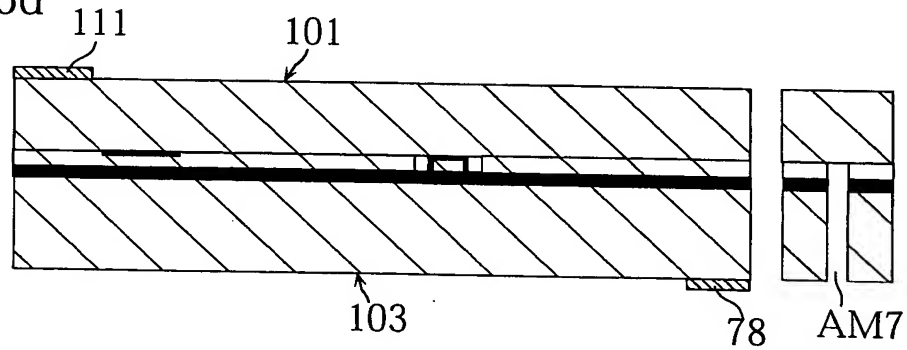


FIG. 27a

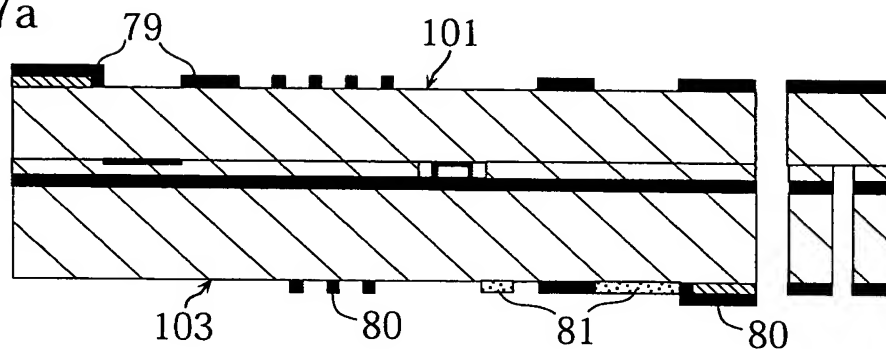


FIG. 27b

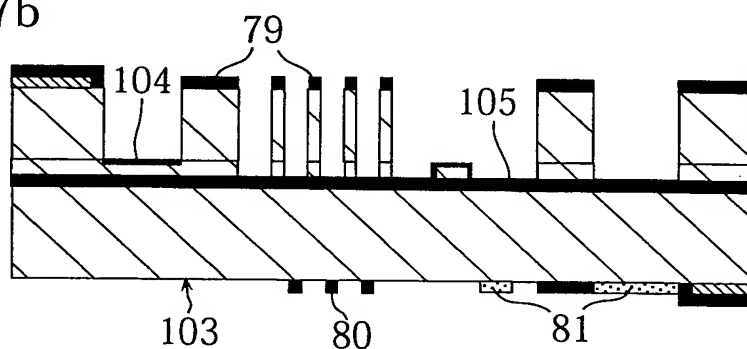


FIG. 27c

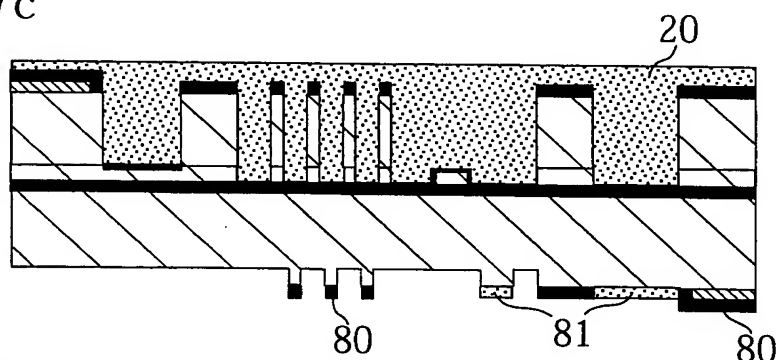


FIG. 27d

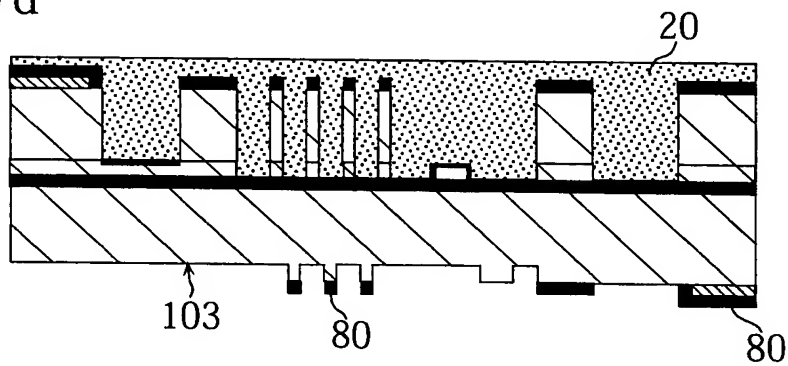


FIG. 28a

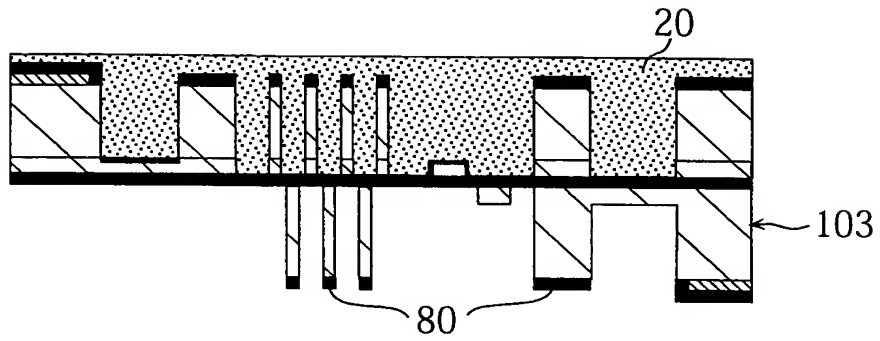


FIG. 28b

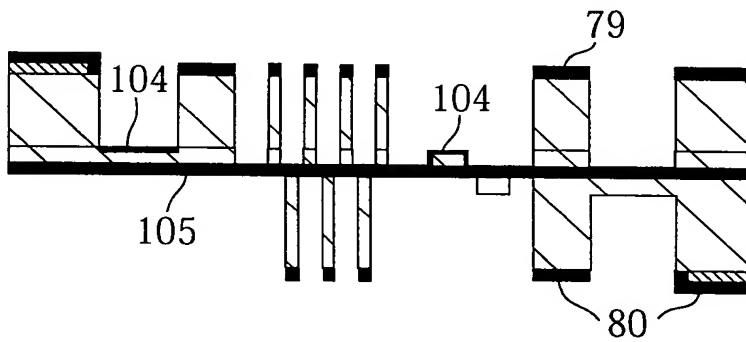


FIG. 28c

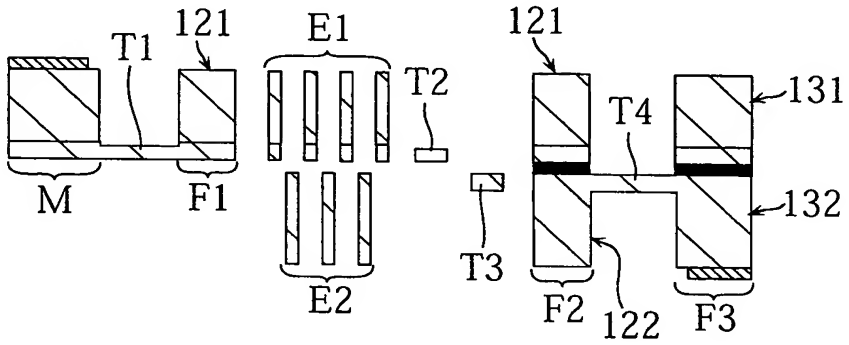


FIG. 30
PRIOR ART

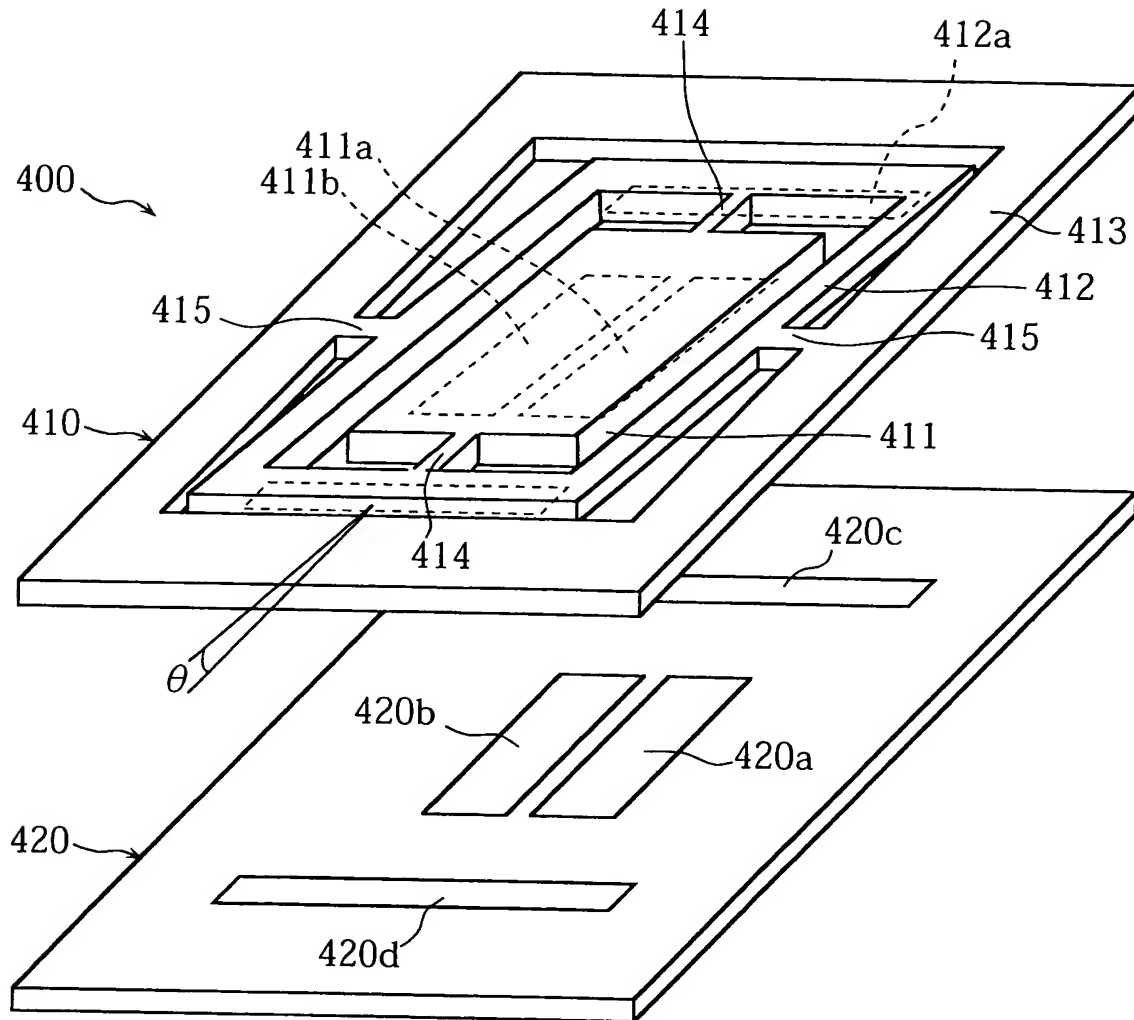


FIG. 32a
PRIOR ART

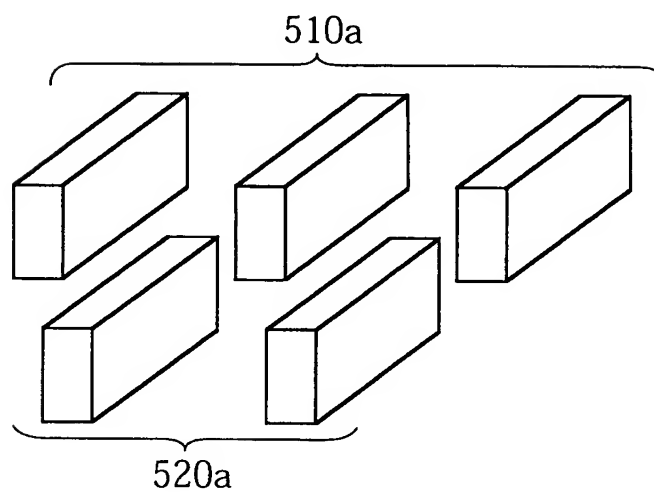


FIG. 32b
PRIOR ART

